**Department of Computer Engineering**

BLG 242E  
Digital Circuits Laboratory Experiment Report

Experiment : 6 Latches and Flip-flops

Experiment Date : 15.04.2016

Group Number : 11

Group Members :

|  |  |  |
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# Introduction

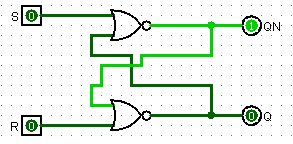
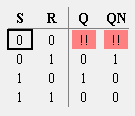
In this experiment, we implemented and examined data storage elements: flip-flops and latches.

# .Requirements

## S-R Latch

We implemented this circuit with the following equipments and ICs:

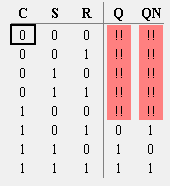
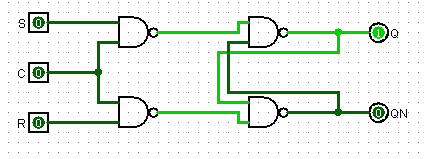
-74xx02 - Quadruple 2-input Positive NOR Gates

## S-R Latch Wıth Enable

We implemented this circuit with the following equipments and ICs:

- 74xx00 - Quadruple 2-input Positive NAND Gates



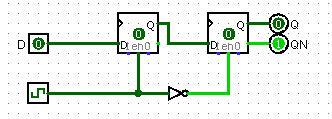
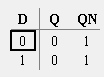
## Negatıve Edge Trıggered D-Flıp Flop

We implemented this circuit with the following equipments and ICs:

- 74xx75 - Quadruple Bistable D Type Latches

- 74xx04 - Hex Inverters

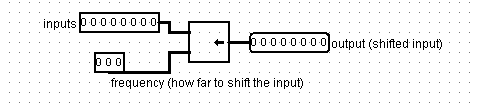
We implemented the circuit on logism with D flip-flops because here was no latches and connected the clock signal with enable input.

## Shıft Regıster

We implemented this circuit with the following equipments and ICs:

-74xx165 - 8-Bit Parallel Input/Serial Output Shift Register



# Conclusion